CLAIMS

What is claimed is:

1. A flash memory source and drain formation process comprising:
depositing a silicide layer in a source and drain area;
implanting a dopant in said source and drain area; and
performing a diffusion process on said source and drain area.

2. The flash memory source and drain formation process of claim 1 wherein said silicide layer comprises cobalt silicide.

3. The flash memory source and drain formation process of claim 1 wherein said dopant comprises arsenic.

4. The flash memory source and drain formation process of claim 1 wherein said diffusion process is performed in a temperature range of about 600 to 950 Celsius.

5. The flash memory source and drain formation process of claim 1 wherein said implanting introduces a dopant into said silicide layer.

6. The flash memory source and drain formation process of claim 5 wherein said dopant in said silicide layer diffuses into said source and drain areas during an anneal process.

7. The flash memory source and drain formation process of claim 1 wherein said source and drain form shallow junctions.

8. A memory cell comprising:
a control gate component having a capacity to receive a charge;
an oxide region having electrical charge insulation characteristics and electrical charge penetration characteristics, said oxide region coupled to said control gate;
a floating gate having a charge trapping region, said floating gate coupled to said oxide region;
a well component having a charge doping characteristic, said well coupled to said floating gate component;
a source component having opposite charge doping characteristics formed by implantation of a dopant and difussion of said dopant from a silicide, said source component coupled to said substrate; and
a drain component having similar doping charge characteristics to said source component and formed by implantation of a dopant and difussion of said dopant from a silicide, said drain component coupled to said substrate.

9. The memory cell of Claim 8 wherein said source and drain form shallow junctions.

10. The memory cell of Claim 8 wherein said source and drain components are configured to reduce leakage current.

11. The memory cell of Claim 8 wherein said source and drain components have reduced resistivity characteristics.

12. The memory cell of Claim 8 wherein said silicide includes cobalt silicide.

13. The memory cell of Claim 8 wherein said dopant includes arsenic.

14. The memory cell of Claim 8 further comprising a sidewall spacer that has a thickness of about 50Å to about 800Å.

15. A flash memory formation method comrpising:
preparing a wafer substrate for lithographic processes;
executing a gate formation process;
performing a silicide source and drain formation process; and
depositing a metal layer over the source and drain respectively.

16. A flash memory formation method of Claim 15 further comprising:
depositing an oxide and a nitride protective layer on said wafer substrate; and
performing a chemical mechanical polishing process.

17. A flash memory formation method of Claim 15 further comprising:
depositing an insulating layer;
creating a floating gate area in said insulating layer;
removing excess charge trapping material;
depositing additional insulating material over said floating gate area;
depositing a control gate material on top of the insulating material;
removing materials deposited during said gate formation process from areas not included under said control gate; and
depositing a sidewall spacer material on the sides of said control gate area.

18. A flash memory formation method of Claim 15 further comprising:
preparing said source and drain area for implantation and diffusion;
depositing a silicide layer in a source and drain area;

implanting a dopant in said source and drain area;

performing a diffusion process on said source and drain area to "push" doping agents included in the silicide layer through the surface of said wafer substrate into said source and drain areas.

19. A flash memory formation method of Claim 15 wherein some of said dopant is trapped in said silicide layer during said implantation of dopants in said source and drain areas.

20. A flash memory formation method of Claim 15 wherein said metal layer couples said source and drain areas to other components included on said wafer.